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Heaslip, et al.
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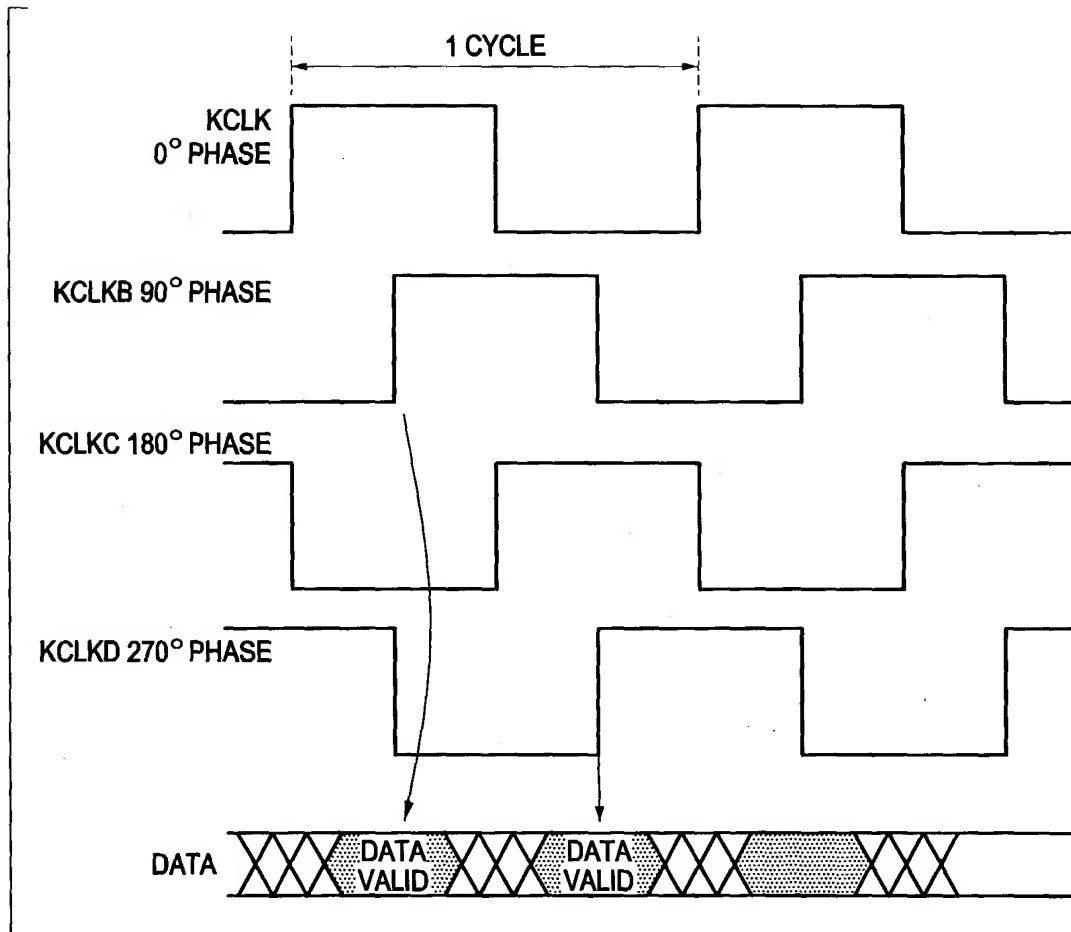
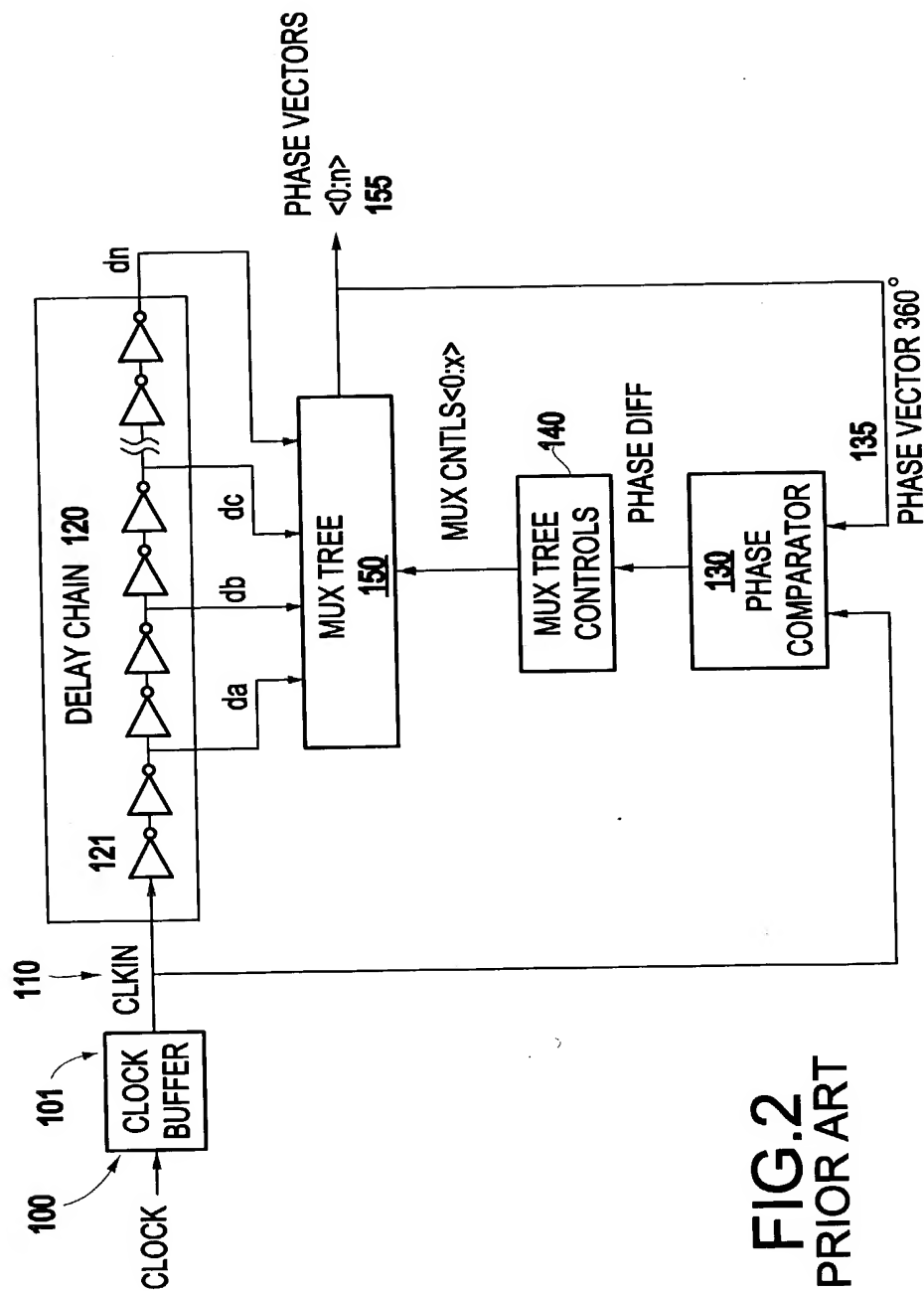
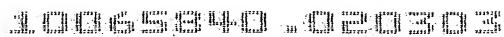


FIG.1



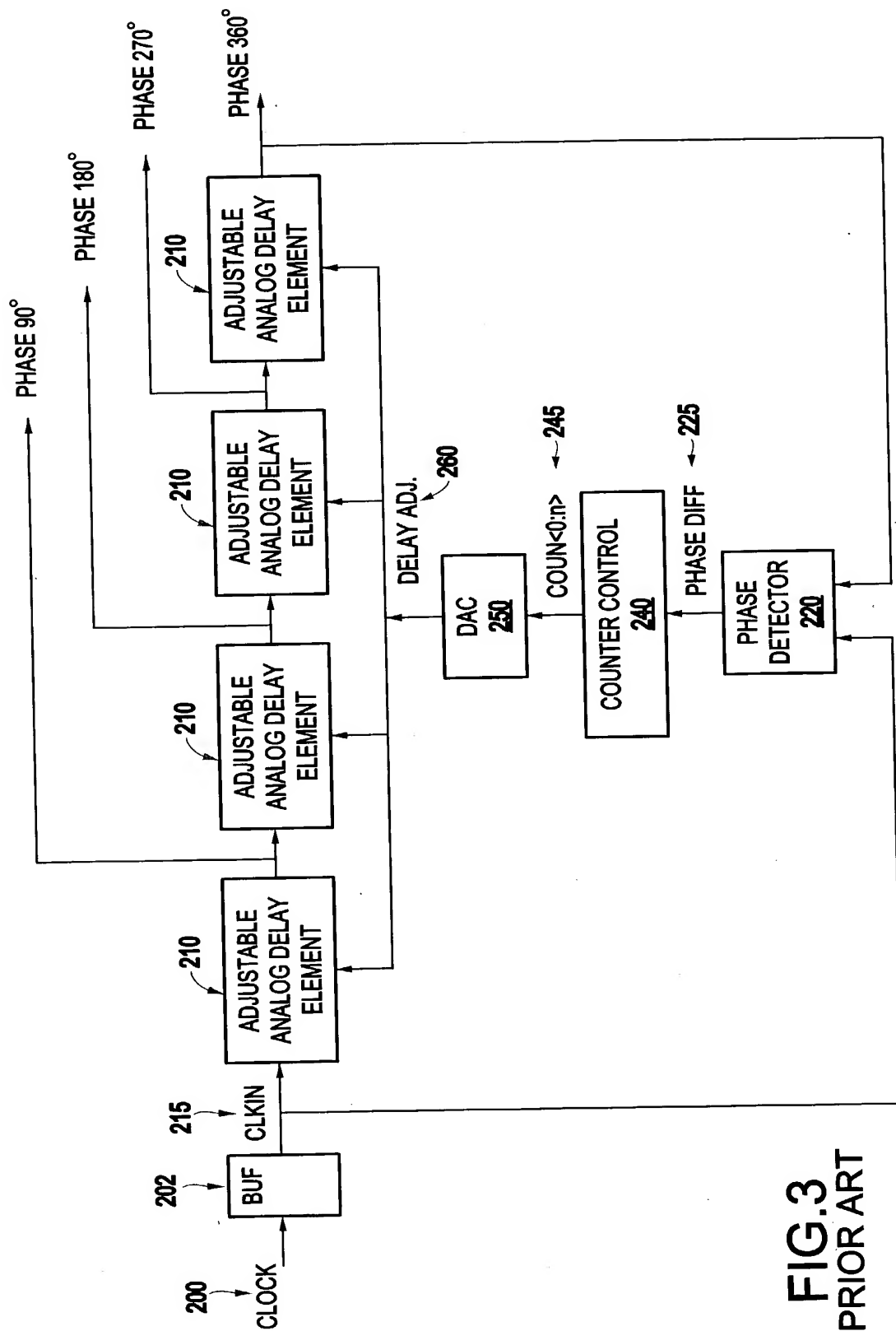


FIG.3
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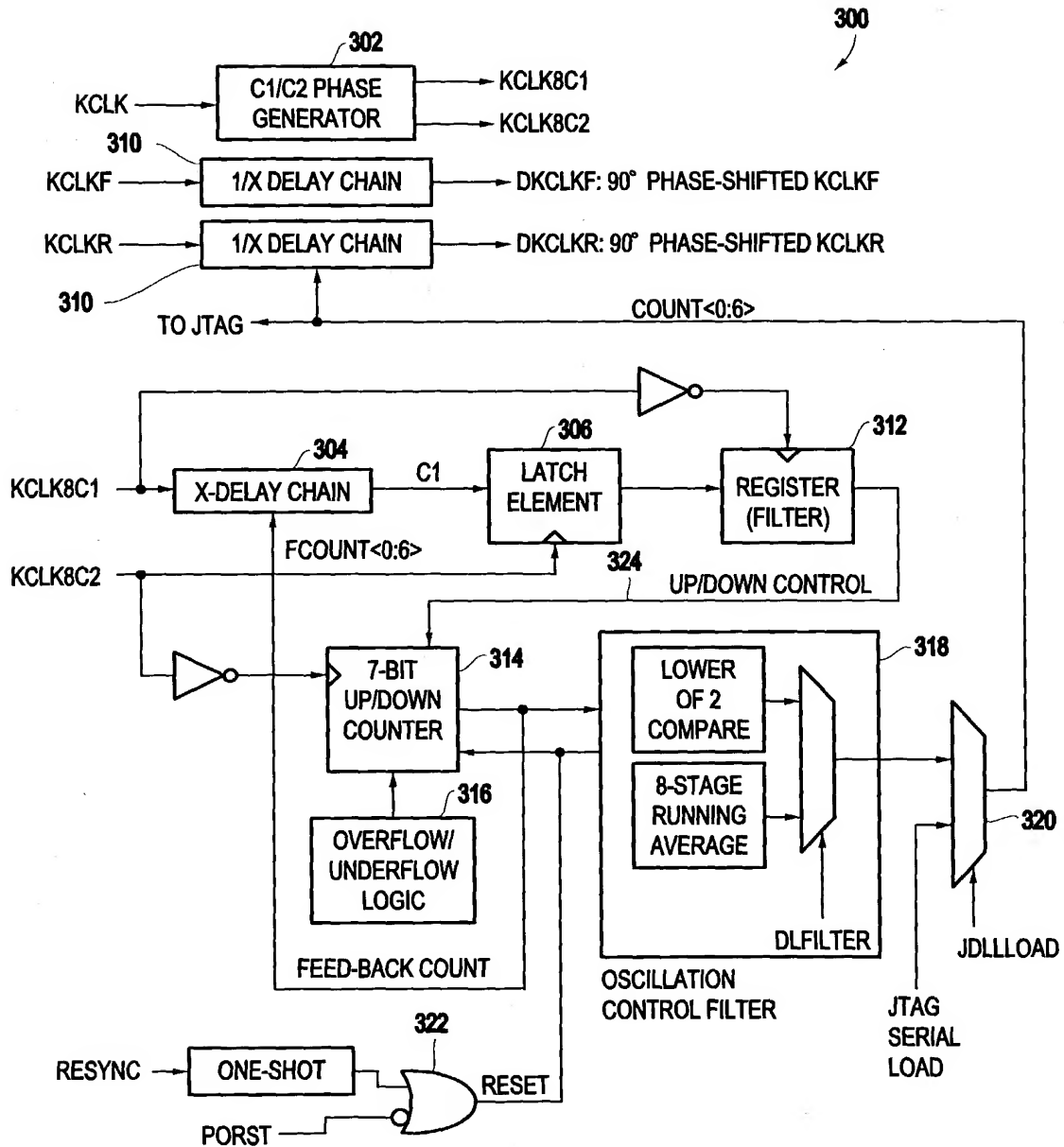


FIG.4



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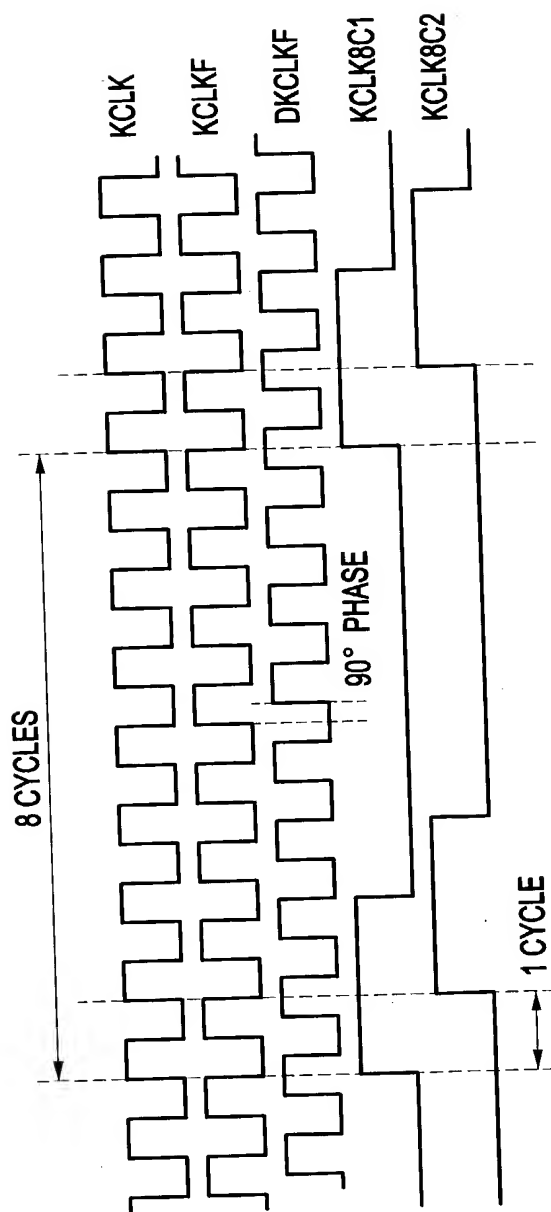
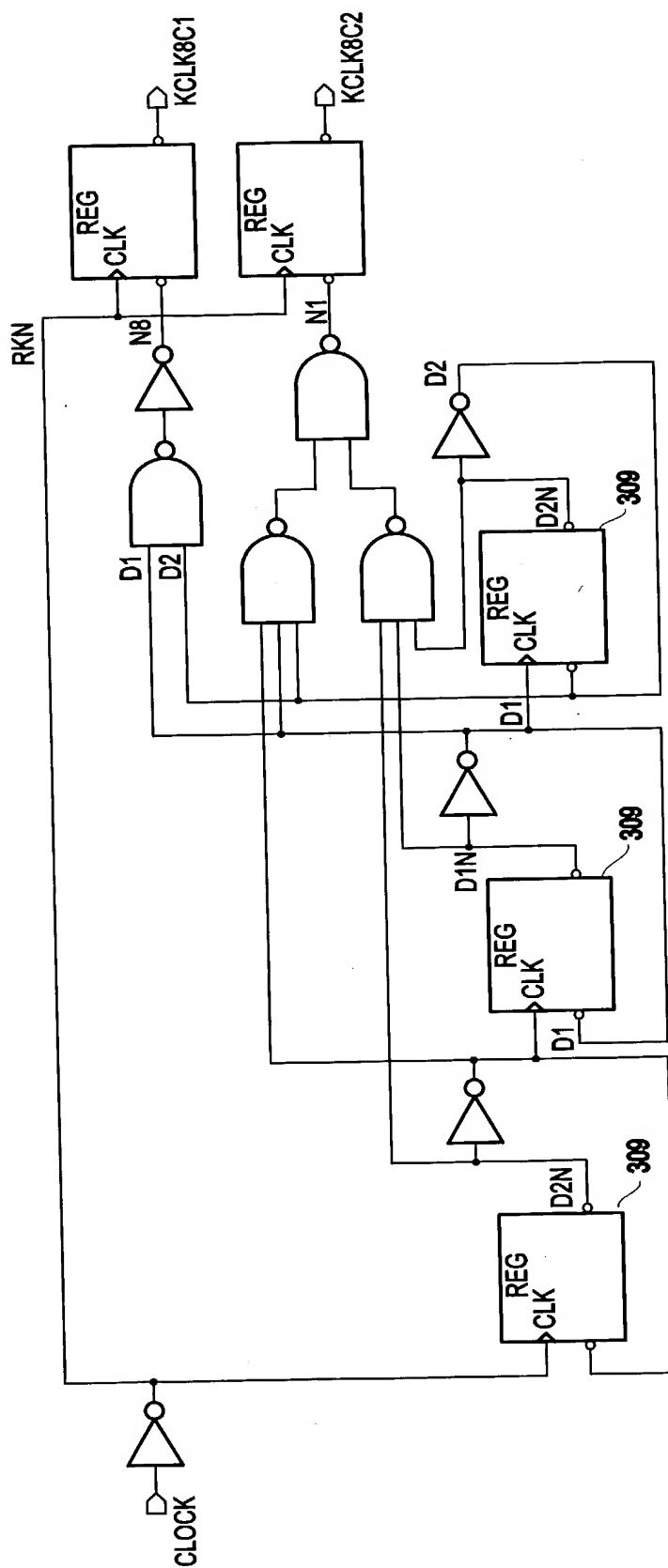


FIG.5



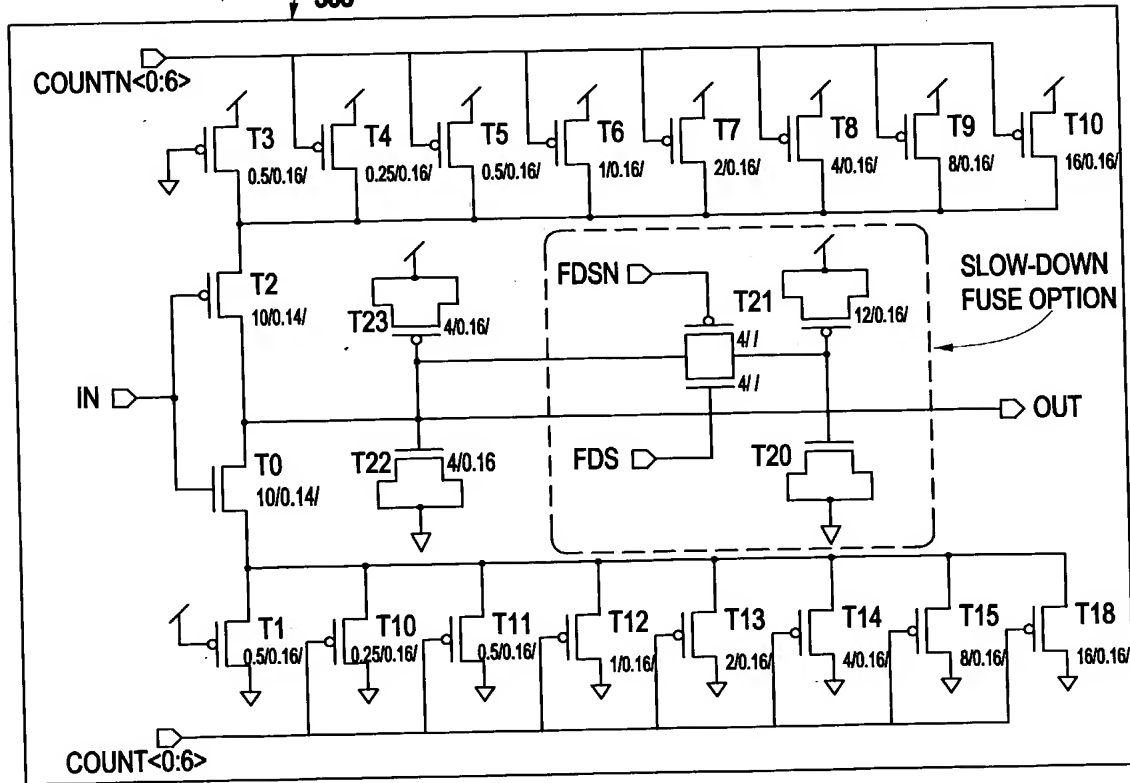
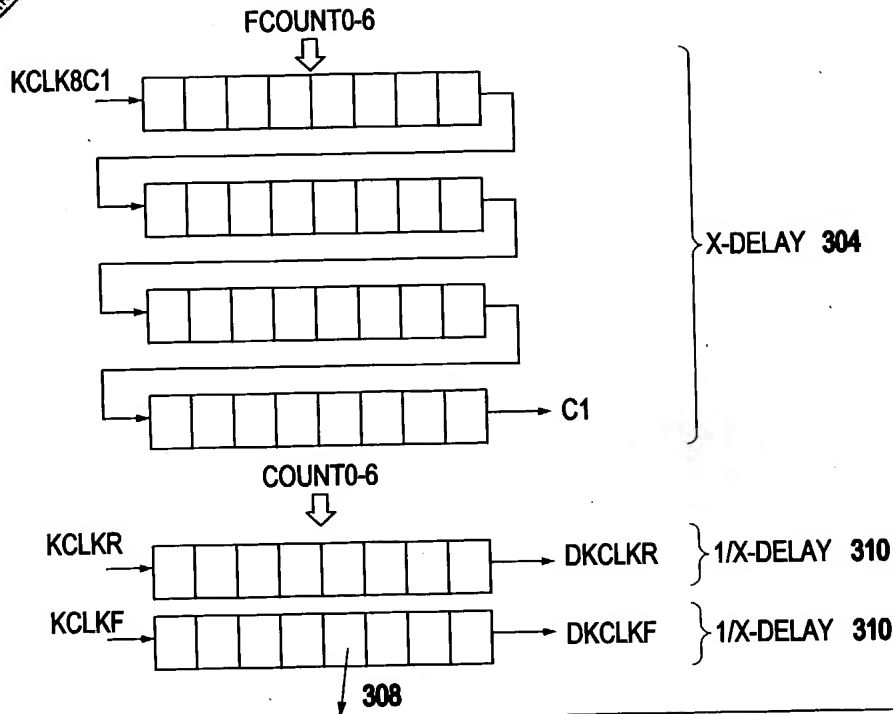


FIG.7

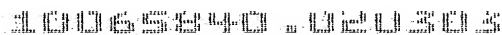


Figure 1 is a block diagram of the KCL8C1 PLL circuit. It shows four cascaded stages of delay elements. Each stage consists of a series of delay elements, some of which are 'DLL X-DELAY ELEMENT 326' (white) and others are '1/X DELAYED-PHASE DELAY ELEMENT 328' (hatched). The stages are labeled KCLK8C1, KCLKR, and C1. The output of the fourth stage is labeled DKCLKR. Arrows indicate the signal flow and feedback paths between the stages and the input/output signals.

FIG.8B



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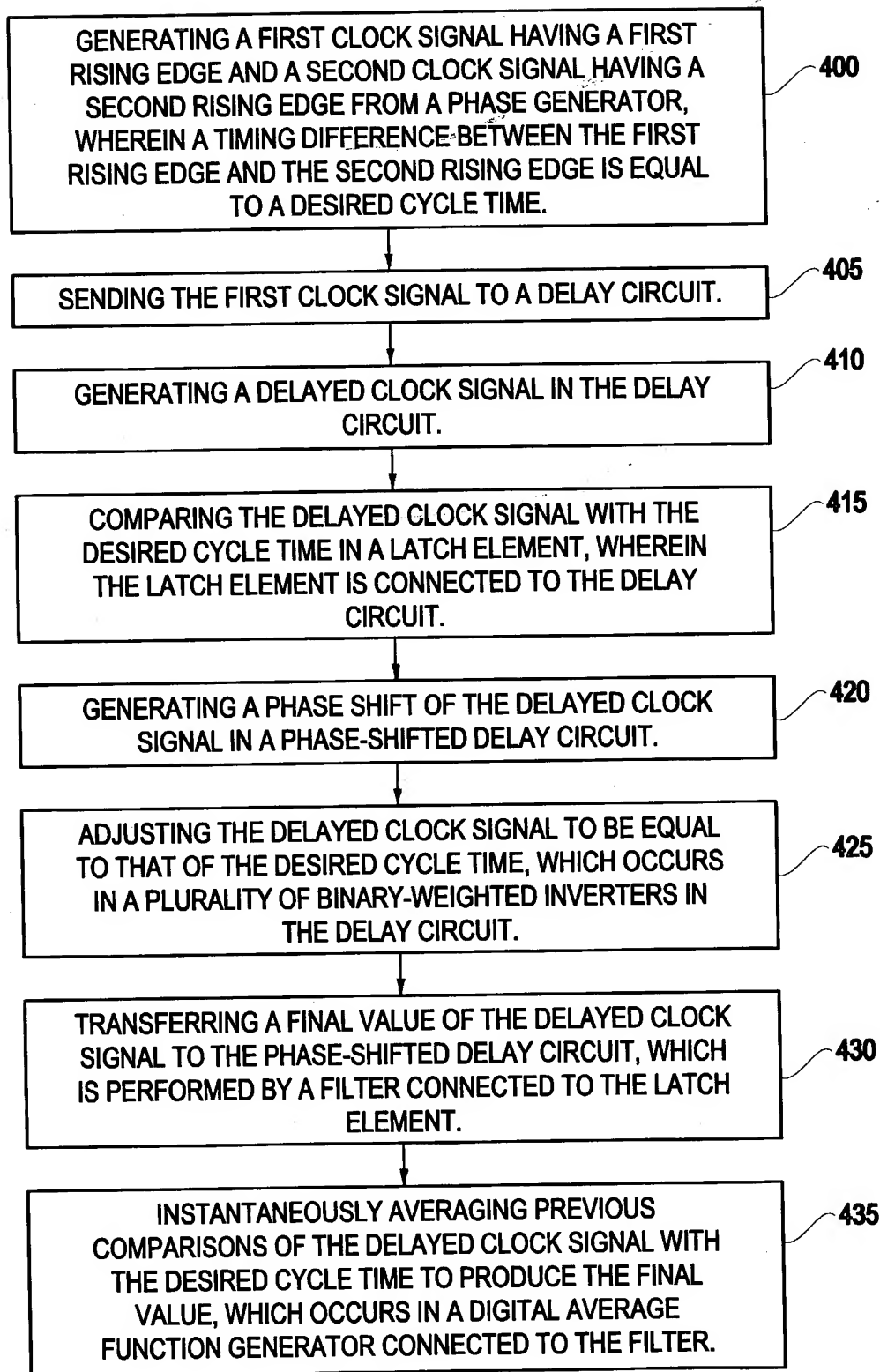
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FIG.9